Remarks

Applicant and his representatives wish to thank Examiner Abraham for repeating the indication that Claims 13-20 are allowed, and for the courteous and helpful discussion held with their representative on June 17, 2005. As discussed, the claims have been amended to obviate the rejection under 35 U.S.C. § 112, first paragraph, and the explanation regarding the patentability of Claims 1-12 and 21-34 over Applicant's "Description of the Related Art" in view of Iwasa, U.S. Pat. No. 6,470,473 [hereinafter "Iwasa"]) is summarized below with reference to the drawings reviewed during the discussion. Other issues discussed (e.g., Applicant's position that the application as filed supports the phrase "scrambled data") are also summarized below.

Claims 1-35 are active in the present application. Claims 1, 3, 5, 7, 9, and 11 have been amended to replace the word "scrambled" with --main--, as originally presented in the claims. Claims 21-25 and 29-32 have been amended for consistency with Claims 1, 3, 5, 7, 9, and 11. Claim 13 is amended to correct an inadvertent typographical error. Thus, no new matter or new issues are introduced by the present Amendment.

The Present Invention

The present invention relates to systems and methods for decoding data. In one embodiment, the system generally comprises a syndrome generator, a data buffer for storing main data and at least a PI syndrome, and an ECC decoder for performing error correction decoding of the main data stored in the data buffer (see Claims 1 and 7 above). In one aspect, the syndrome generator generates PI and PO direction syndromes, the ECC decoder uses the PI and PO syndromes for error correction decoding, and the system also comprises a memory that stores the PO direction syndrome during its generation (Claim 1). In another aspect, the ECC decoder error correction decodes the PI syndrome and the PO (Claim 7).

In another embodiment, the method for decoding data comprises demodulating the data to generate an ECC (Error Correction Code) block that comprises main data, a PI, and a PO; calculating at least a PI direction syndrome; writing at least the main data and PI direction

syndrome into the data buffer; performing error correction decoding of the PI and PO directions; and when errors are found, correcting the PI direction syndrome and the PO direction syndrome, and writing corrected main data into the data buffer (see Claims 5 and 11 above). In one aspect, the method further comprises calculating the PO direction syndrome, storing PO direction syndrome data in a memory during such calculating, and reading the PI and PO direction syndromes from the data buffer to an ECC decoder (Claim 5). In another aspect, the PO is written into the data buffer, the PO is read from the data buffer to an ECC decoder to calculate a PO direction syndrome (Claim 11).

Thus, as shown in Exhibit A-1 attached hereto, the present invention includes syndrome generator, a data buffer for storing main data and at least a PI direction syndrome (generated by the syndrome generator), and an ECC decoder for error correction decoding the main data (stored in the data buffer). The technology in Applicant's "Description of the Related Art" does not include a syndrome generator or a data buffer for storing at least a PI direction syndrome (see Exhibit A-1, "Applicant's Fig. 1"). Iwasa generally discloses a decoding process and system that error correction decodes data before transferring it to a buffer of sufficient size to store the error correction decoded data. As a result, Iwasa discloses a different architecture from that disclosed in Applicant's "Description of the Related Art" or recited in the present claims. Thus, although Iwasa discloses a syndrome generator block and a memory block for storing a generated syndrome (see Exhibit A-1, "Iwasa"), the different architecture disclosed by Iwasa introduces complications and complexities not associated with the architecture of Applicant's "Description of the Related Art" or the present invention (as will be explained below). Thus, one of ordinary skill in the art would not look to the Iwasa for modifications to the decoder architecture of Applicant's Fig. 1. Consequently, Iwasa is not properly combinable with Applicant's "Description of the Related Art" to render the present invention obvious, because the differences in the architectural approaches of Applicant's "Description of the Related Art" and Iwasa cannot be ignored. However, even if one could combine Iwasa with Applicant's "Description of the Related Art," the combination does not suggest or lead one to the improvements provided by the present invention. Thus, the present claims are patentable over the combination of Applicant's "Description of the Related Art" and Iwasa.

The Rejection of Claims 1-12 and 21-33 under 35 U.S.C. § 103(a)

The rejection of Claims 1-12 and 21-33 under 35 U.S.C. § 103(a) as being unpatentable over Applicant's "Description of the Related Art" in view of Iwasa is respectfully traversed.

As explained in the Amendment dated January 21, 2005, Applicant has not, at any time, admitted that the section of the present application entitled "Description of the Related Art" (Applicant's "Description of the Related Art") is actually prior art that is available against the present claims under any section of 35 U.S.C. § 102 et seq. However, Applicant and his undersigned representative simply stand on their prior argument in the Amendment dated January 21, 2005, and reserve further argument on this issue for later, should it become necessary to do so.

However, assuming for the sake of argument that the technology disclosed in Applicant's "Description of the Related Art" is available as prior art against the present claims, Applicant's "Description of the Related Art" and FIG. 1 relate to a decoder architecture and method that simply store main data and PI and PO information in a data buffer, then ECC decoding and syndrome generation are performed later (also see Exhibit A-1 attached hereto). In this architecture, the ECC decoder must access the main data buffer at least twice for error correction decoding (reading data from the buffer and calculating the syndrome in a given direction, then writing corrected data back into the buffer), separately for each of the PI direction and in the PO direction (p. 2, ll. 34-39 and 46-48, and p. 3, ll. 65-69).

By contrast, the present invention includes a syndrome generator that generates at least a PI syndrome and a data buffer that stores main data and at least a PI syndrome. In one embodiment (Claim 1, exemplified by Fig. 4 of the present application and shown in Exhibit A-1 attached hereto), the syndrome generator generates a PI syndrome and a PO syndrome, the system further includes a memory for storing the PO syndrome during its generation, and the data buffer stores main data and the PI and PO syndromes. Referring now to Claim 1 and the attached Exhibit A-1, by storing the PI and PO syndromes in the data buffer with main data, the ECC decoder only needs to read the PI and PO syndromes from the data buffer to perform error correction decoding in both directions before writing corrected syndromes and the corrected part

of the main data back into the buffer (p. 6, l. 180 - p. 7, l. 185), enabling abandonment of the PI and PO after generating the PI and PO syndromes. Another important benefit achieved is that data buffer access times are reduced, since reading the main data from or writing the entire main data back to the data buffer before and after decoding is no longer required (p. 7, ll. 185-190 and 201-209).

In a further embodiment (Claim 7, exemplified by Fig. 6 of the present application), the syndrome generator generates a PI syndrome, and the data buffer stores main data and the PI syndrome, but the system is not required to have a memory for storing the PO syndrome. Thus, in the case of Claim 7, by storing the PI syndrome in the data buffer with main data and the PO, the ECC decoder can read the PI syndrome from the data buffer and write the corrected PI syndrome, and corrected part of the main data and PO into the buffer (p. 8, ll. 231-232). Of course, in the case of Claim 7, to enable complete correction of the main data, the ECC decoder reads the main data and the PO from the buffer when performing error correction decoding in the PO direction (but not necessarily the PI syndrome, which the ECC decoder does not need for error correction in the PO direction), then writes corrected PI syndrome and the corrected part of the main data back into the data buffer (p. 8, ll. 231-232). Thus, even in the case of the present Claim 7, data buffer access times are still reduced relative to Applicant's "Description of the Related Art" and FIG. 1 (p. 8, ll. 239-240), as the main data does not need to be read out from the data buffer for PI direction decoding. Thus, both the present Claims 1 and 7 provide advantages over the architectures of Applicant's "Description of the Related Art"/FIG. 1 and Iwasa, at least in part by enhancing the parallel processing capability of the decoding system (see p. 3, ll. 74-77).

Neither FIG. 1 nor Applicant's description thereof discloses a syndrome generator for generating at least a PI direction syndrome from an ECC block as recited in Claims 1 and 7 (or the step of generating a PI direction syndrome as recited in Claims 5 and 11). Also, neither FIG. 1 nor Applicant's description thereof discloses a data buffer for storing at least a PI direction syndrome along with main data as recited in Claims 1 and 7 (or the step[s] of writing main data and at least a PI direction syndrome into such a data buffer as recited in Claims 5 and 11). Thus,

assuming for the sake of argument that the technology disclosed in Applicant's "Description of the Related Art" is available as prior art against the present claims, Applicant's "Description of the Related Art" and Applicant's FIG. 1 are saliently deficient with respect to the presently claimed invention.

Iwasa fails to cure the salient deficiencies of Applicant's "Description of the Related Art." Iwasa discloses a DVD-ROM data decoding processing system, including a DVD-ROM reproducing unit 32 and a buffer memory 34 (Abstract, ll. 1-2 and FIG. 3). The DVD-ROM reproducing unit 32 includes a demodulating part 36, a PI syndrome generating part 38, an error correcting part 40, a buffer memory 42 having a memory capacity corresponding to a few lines, a PO syndrome generating part 44, a descrambling/EDC calculating part 46, a PI syndrome storing memory 48, a PO syndrome storing memory 50, an EDC calculation result storing memory 52, an error correcting part 54, and a CPU 56 (Abstract, ll. 3-10 and FIG. 3). The error correcting part 40 derives the position and the magnitude of errors in the PI series from the PI syndromes generated in the PI syndrome generating part 38, and corrects the data errors in the buffer memory 42 on the basis of the position and the magnitude of errors in the PI series, interleave by interleave (Abstract, ll. 10-15). The error correcting part 54 reads out the PO syndromes of one block from the PO syndrome storing memory 50, to derive the position and the magnitude of errors in the PO series, and to correct the data errors in the buffer memory 34 on the basis of the position and the magnitude of errors in the PO series thus derived (Abstract, ll. 16-21).

Buffer memory 42 of Iwasa has a memory capacity corresponding to only a few lines (col. 4, ll. 16-17). Thus, buffer memory 42 stores only a few lines of demodulated data (col. 4, ll. 16-17), as opposed to main data from an ECC block and at least a PI direction syndrome, as recited in the present Claims 1 and 7. Furthermore, PI syndrome storing memory 48 of Iwasa receives either PI syndromes generated in the PI syndrome generating part 38 or, if data error(s) in the buffer memory 42 have been corrected, a syndrome of "0" (col. 4, l. 61-col. 5, l. 2). Thus, PI syndrome storing memory 48 clearly stores at most only the PI syndrome, and no main data (see col. 4, l. 66-col. 5, l. 8 and FIG. 6). By contrast, the present Claims 1 and 7 recite a data buffer for storing scrambled data from an ECC block and at least a PI direction syndrome.

Buffer memory 34 is the only buffer disclosed by Iwasa that can store a block of data. It receives and develops descrambled data from the descrambling/EDC calculating part 46 (col. 5, ll. 12-17 and FIG. 3). Thus, buffer memory 34 of Iwasa appears not to store a PI syndrome, PO syndrome, or PO (see, e.g., col. 5, l. 45-col. 6, l. 9, and col. 6, ll. 42-59 of Iwasa). As a result, none of the buffers/memories disclosed by Iwasa stores main data from an ECC block and at least a PI direction syndrome, as recited in the present Claims 1 and 7. Furthermore, Iwasa is silent with regard to writing main data and at least a PI direction syndrome into such a data buffer (see amended Claims 5 and 11) because error correcting decoding has been performed before data storage, and therefore, PI or PO direction syndrome is no longer required at the time when storing the data into Iwasa's buffer memory 34. Thus, Iwasa does not cure the deficiencies of Applicant's "Description of the Related Art" with regard to the present claims.

Furthermore, referring to Exhibit A-1, Iwasa has a decoding architecture reversed from that of Applicant's "Description of the Related Art," in that error correction (ECC decoding) is performed before main data is stored in a data buffer of sufficient size to store it (the "ECC before buffer" architecture). While it is true that Iwasa discloses a syndrome generator and a memory upstream of the data buffer, placing the ECC decoder upstream of the data buffer (as Iwasa does) requires that the syndrome generator and memory are also upstream of the ECC decoder, thereby imposing certain complexities and functional requirements on the upstream circuitry in the "ECC before buffer" architecture that are not necessarily part of the "buffer before ECC" architecture of Applicant's Fig. 1. Thus, one of ordinary skill in the art would not look to the "ECC before buffer" architecture of Iwasa when modifying the "buffer before ECC" architecture of Applicant's Fig. 1.

Even further, the complexities and functional requirements associated with placing the syndrome generator upstream of the ECC decoder in the "ECC before buffer" architecture of Iwasa are not required by the present invention. Thus, assuming one would of ordinary skill in the art would look to the "ECC before buffer" architecture of Iwasa when modifying the "buffer before ECC" architecture of Applicant's Fig. 1, the relative structural and functional simplicity

of the present invention would not be readily apparent to one of ordinary skill in the art from a reading of Applicant's "Description of the Related Art" and Iwasa.

For example, when an ECC block contains main data, a PI and a PO, it is known in the art that complete error correction decoding is performed in both the PI and PO directions (see, e.g., p. 1, l. 14 - p. 2, l. 48 of the present application; and col. 1, ll. 10-22 and 48-52, and col. 2, ll. 53-57 of Iwasa). Thus, as shown in the attached Exhibit A-2, Iwasa generates both the PI and PO syndromes before ECC decoding (col. 2, ll. 53-57). However, Iwasa has to store the syndromes somewhere in order to error correct the data in both directions and to repeat error correction (which is necessary when performing an error detection code calculation to confirm that the data have no error; see, e.g., col. 3, ll. 7-40 of Iwasa). As a result, according to the above-cited passages of Iwasa and as shown in the attached Exhibit A-3, the PI and PO syndromes each have a separate memory for storing the syndrome once it is generated, and also, a third memory upstream of the ECC decoder must be present to store the data temporarily while the PO syndrome is being calculated. (Iwasa takes advantage of the stored PI syndrome to error correct the data before generating the PO syndrome, but this detail is not particularly relevant to the discussion of the present claims.) Thus, the "ECC before buffer" architecture of Iwasa requires a certain structural and functional complexity on the circuitry upstream of the ECC decoder and main data buffer.

The level of complexity required by the "ECC before buffer" architecture of Iwasa is not required by the "buffer before ECC" architecture of Applicant's Fig. 1. As explained above, the PI and PO can be stored in the buffer of Applicant's Fig. 1, and the ECC decoder can access the data buffer as needed to obtain the PI or PO, generate a syndrome therefrom, correct data (including the PI or PO), and write the corrected data and parity information (PI or PO) back into the buffer. Thus, the architectural differences between the "ECC before buffer" architecture of Iwasa and the "buffer before ECC" architecture of Applicant's Fig. 1 would not motivate or lead one of ordinary skill in the art to look to Iwasa for desirable modifications of Applicant's Fig. 1.

Furthermore, there does not appear to be any suggestion or indication in either Applicant's "Description of the Related Art" or Iwasa that placing a syndrome generator (and

optional memory for storing a PO syndrome during its generation) before a data buffer in a "buffer before ECC" architecture will lead to reduced architectural complexity (relative to Iwasa), reduced access times (relative to Applicant's Fig. 1), or enhanced parallel processing capability (relative to both Applicant's Fig. 1 and Iwasa). The reduced access times and relative structural simplicity are discussed above, and will not be repeated here. However, it is reasonably clear from the attached Exhibits that neither Applicant's Fig. 1 (which performs all syndrome generation and ECC decoding after the main data are stored in the buffer) nor Iwasa (which performs all syndrome generation and ECC decoding before the main data are stored in the buffer) teach, suggest or contemplate enhancing the decoding system's parallel processing capability by performing part or all of the syndrome generation before storing main data in the buffer and performing ECC decoding after storing main data in the buffer (see, e.g., p. 3, ll. 74-77 of the present specification). For example, it is believed that the PI and PO decoding processes of Iwasa are limited (e.g., by processing speed and/or syndrome memory size) because the decoding process for a given block has to be completed before the arrival of the next block in order to prevent a buffer overflow condition.

Consequently, even if one assumes that details of the "ECC before buffer" architecture of Iwasa would be used to modify the "buffer before ECC" architecture of Applicant's Fig. 1, the reduced access times, relative structural and functional simplicity, and enhanced parallel processing capability of the present invention would not be readily apparent to one of ordinary skill in the art from a reading of Applicant's "Description of the Related Art" and Iwasa.

As a result, the present invention is fully patentable over Applicant's "Description of the Related Art" in view of Iwasa. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 1-12 and 21-33 under 35 U.S.C. § 112, First Paragraph

The rejection of Claims 1-12 and 21-33 under 35 U.S.C. § 112, first paragraph, has been overcome by appropriate amendment.

Nonetheless, to ensure that the record is clear, the present application clearly supports the phrase "scrambled data." As stated in the Amendment filed January 21, 2005, the specification discloses that the de-scrambler and EDC check (e.g., 116 in FIG. 4 and 804 in FIG. 8) read the data stored in the data buffer to de-scramble the main data and check whether errors are corrected (p. 7, lines 190-194 and p. 10, lines 281-283). Logically, the data stored in the data buffer can be de-scrambled only if it is scrambled. In addition, the application clearly and repeatedly discloses decoding data from an optical or DVD storage device, which can be a disk (p. 1, ll. 14-16; p. 2, ll. 32-33; p. 3, ll. 78-79; and p. 10, ll. 299-300).

It is well-known in the art that digital video data use NRZI code and a scrambler to improve receiver clock recovery (see Iwasa, col. 1, ll. 10-22, and Robin et al., "Digital Television Fundamentals," 2nd ed., McGraw-Hill, New York, New York (2000), p. 286, last paragraph and p. 288, first paragraph; submitted herewith). The original data are recovered using an NRZI-to-NRZ converter and a descrambler (Robin et al., p. 288, the last paragraph of section 7.2). A diagram of such a descrambler explicitly operating on scrambled data is shown in Figure 7.5 of the Robin et al. text (p. 290). Furthermore, Fig. 7-17 (p. 301) of Robin et al. shows the operation of a descrambler on a serial data input as part of a larger deserializer, and describes the functionality of the descrambler with respect to section 7.2 (see p. 302). Thus, even though the serial data input in Fig. 7-17 of Robin et al. is not specified as being scrambled, one skilled in the art would understand that it is scrambled because the descrambler is operating on it.

In addition, it is well-known in the art that encryption is widely used to protect the content of pre-recorded DVD video disks (see Taylor, "DVD Demystified," 2nd ed., McGraw-Hill, New York, New York (2001), p. 481, last 3 full paragraphs). When an encrypted sector is encountered, the DVD drive and the decoder exchange a set of keys that eventually produces the key used by the decryptor to decrypt the data (see Taylor, p. 482, lines 3-7), and that encrypted

content must be decrypted before a decoder can process it (see the sentence bridging pp. 482-3). Taylor highlights a "NOTE" on p. 482 that in this context, "scrambling" and "encryption" mean the same thing. From these passages and the decryption section on pp. 483-5, one skilled in the art would understand that a decryption module (or descrambler) descrambles scrambled data.

Thus, the present application supports the phrase "scrambled data." As such, use of the term "scrambled data" in the Amendment filed January 21, 2005 is not new matter. However, to advance prosecution as efficiently as possible, Applicant has amended the claims to change "scrambled data" back to --main data--, as requested by the Examiner at the discussion on June 17, 2005.

Conclusions

In view of the above amendments and remarks, all bases for rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

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